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| 09/632,662 | 08/04/2000 | Jeff S. Ford | 1247/A53 | 2282 | |
| 22801 | 7590 12/18/2002 | | | | |
| LEE & HAYES PLLC | | | EXAMINER | | |
| SPOKANE, | RSIDE AVENUE SUITE : WA 99201 | 500 | LO, LINUS H | | |
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| | | | 2614 | * | |
| | | | DATE MAILED: 12/18/2002 | | |

Please find below and/or attached an Office communication concerning this application or proceeding.

| | Application | on No. | Applicant(s) | | | | | |
|---|----------------|------------------------|---|----------|--|--|--|--|
| | 09/632,66 | 2 | FORD ET AL. | | | | | |
| Office Action Summary | Examiner | | Art Unit | | | | | |
| | Linus H L | | 2614 | | | | | |
| The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply | | | | | | | | |
| A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). - Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b). Status | | | | | | | | |
| 1) Responsive to communication(s) filed on | | | | | | | | |
| 2a) This action is FINAL . 2b) ☑ Th | nis action is | non-final. | • | | | | | |
| 3) Since this application is in condition for allow | | | | erits is | | | | |
| closed in accordance with the practice under Disposition of Claims | Ex parte Q | uayle, 1935 C.D. 11, 4 | 53 O.G. 213. | | | | | |
| 4) Claim(s) 1-33 is/are pending in the application | | | | | | | | |
| 4a) Of the above claim(s) is/are withdra | wn from cor | nsideration. | | | | | | |
| 5) Claim(s) is/are allowed. | | | | | | | | |
| 6)⊠ Claim(s) <u>1-33</u> is/are rejected. | | | | | | | | |
| 7) Claim(s) is/are objected to. | | | | | | | | |
| 8) Claim(s) are subject to restriction and/o | or election re | equirement. | | | | | | |
| Application Papers | | | | | | | | |
| 9) The specification is objected to by the Examine | | | , the Eveniner | | | | | |
| 10) The drawing(s) filed on <u>04 August 2000</u> is/are: a) accepted or b) objected to by the Examiner. | | | | | | | | |
| Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a). 11) The proposed drawing correction filed on is: a) approved b) disapproved by the Examiner. | | | | | | | | |
| If approved, corrected drawings are required in reply to this Office action. | | | | | | | | |
| 12) The oath or declaration is objected to by the Examiner. | | | | | | | | |
| Priority under 35 U.S.C. §§ 119 and 120 | | | | | | | | |
| 13) Acknowledgment is made of a claim for foreig | n priority un | der 35 U.S.C. § 119(a |)-(d) or (f). | | | | | |
| a) ☐ All b) ☐ Some * c) ☐ None of: | | • | | | | | | |
| 1. Certified copies of the priority document | ts have bee | n received. | | | | | | |
| 2. Certified copies of the priority documents have been received in Application No | | | | | | | | |
| 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. | | | | | | | | |
| 14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application). | | | | | | | | |
| a) The translation of the foreign language provisional application has been received. 15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121. | | | | | | | | |
| Attachment(s) | ao priority di | 120, 00 0.0.0. 33 120 | una/or 121. | | | | | |
| 1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO-1449) Paper No(s) | · | | (PTO-413) Paper No(s) Patent Application (PTO-15 | | | | | |
| | | | | | | | | |

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DETAILED ACTION

Claim Rejections - 35 USC § 112

- 1. Claim 33 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.
- 2. Claim 33 recites the limitation "The system according to claim 17 means for removing" in lines 1-2. There is insufficient antecedent basis for this limitation in the claim. It is noted the preceding parent claim is a method claim and no such system has been claimed. Therefore the claim rendered indefinite for the scope of the claim. Appropriate correction is required.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.
- 2. Claims 1, 3, 4, 6-8, 15-17, 19, 20, 22-24, and 31-32 are rejected under 35 U.S.C. 102(e) as being anticipated by Wang et al. '906.

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Considering claim 1, Wang et al. multiple pipeline memory controller for servicing real time data. Wang et al. discloses the following limitations a video input system for preprocessing video signals, note:

- a) the claimed video input system for pre-processing video signals which is met by the video graphic controller VGC 26 with a multiple pipeline (Fig. 2, column 3, lines 24-26 and lines 38-43);
- b) the claimed video input module for receiving and forwarding one or more live video signal, the video input module producing a forwarded video signal for each received live video signal which is met by the video capture controller 38 (Fig. 2, column 3, lines 38-43);
- the claimed first video pipeline for pre-processing VS_1 , wherein VS_1 is a first stored video signal or one of the forwarded video signals produced in the video input module, the first video pipeline producing a first pre-processed video signal which is met by the pipeline processor 68 (Fig. 3, column 4, lines 5-9, column 3, lines 60-65), whereas passage from column 4 describes pipeline processor 68 receives and processes the real time input signal from port 64, while the passage from column 3 additionally describes that the real time signal (VS_1) at port 64 which is the video capture signal originated from the video capture controller 38 (video input module); and
- d) the claimed second video pipeline for pre-processing Vs2, wherein Vs2 is the same video signal being pre-processed in the first video pipeline, one of the other forwarded video signals produced in the video input module, or a second stored video signal, the second video pipeline producing a second pre-processed video signal which

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is met by the other dual pipeline processor 70 (Fig. 3, column 4, lines 2-15, column 3, lines 54-58), whereas the excerpt from column 4 describes that an non-real time signal is input thru the input port 66 to the other dual pipeline processor 70, while excerpt from column 3 describes that the input non-real time signal is generated by the GUI engine and retrieved from the accesses memories (a second stored video signal).

Considering claim 3, the claimed limitation of wherein the received live video signal is VS, wherein the VS is an analog composite video signal, ... or a parallel digital component video signal which is met by the description at column 3, lines 38-43, whereas the described CATV signal is the analog composite video signal.

Considering claim 4, the claimed limitation of wherein the formatted video signal includes D, wherein D is color data, alpha data or color and alpha data which is met by the description at column 3, lines 38-43, whereas the described CATV signal contain color data.

Considering claim 6, the claimed limitation of wherein the first pre-processed video signal is output to a storage medium which is met by the memory 60 (column 4, lines 28-36), whereas the described pipeline processor 68 (first pre-processor) forward an output signal to memory 60, and the claimed second pre-processed video signal is forwarded to a video graphics processor which is met by the description of video overlay engine 52 at column 3, lines 45-53, whereas the overlay engine 52 requested an non-real time signal from the pipeline processor that is contained within the pipeline memory controller 28 (Fig. 3), and the engine 52 generate

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an video image that overlay the video information (real time signal) on graphics, non real time signal (second pre-processed video).

Considering claim 7, note:

- a) the claimed limitation of wherein the first pre-processed video signal is output to a storage medium which is met by the memory 60 (column 4, lines 28-36), whereas the described pipeline processor 68 (first pre-processor) forward an output signal to memory 60; and
- b) the claimed second pre-processed video signal is forwarded to a video output system which is met by the description of video overlay engine 52 and the screen 50 at column 3, lines 45-53, whereas the overlay engine 52 requested an non-real time signal from the pipeline processor that is contained within the pipeline memory controller 28 (Fig. 3), and the engine 52 generate an video image that overlay the video information (real time signal) on graphics, non real time signal (second pre-processed video).

Considering claim 8, note:

a) the claimed limitation of wherein the first pre-processed video signal is forwarded to a video graphic processor which is met by the CRT controller 46 (Fig. 2 column 3, lines 43-46, whereas the real time signal (first pre-processed video signal) is inherently processed for rendering the signal to be display by the CRT screen; and

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b) the claimed second pre-processed video signal is forwarded to a video output system which is met by the description of video overlay engine 52 and the screen 50 at column 3, lines 45-53, whereas the overlay engine 52 requested an non-real time signal from the pipeline processor that is contained within the pipeline memory controller 28 (Fig. 3), and the engine 52 generate an video image that overlay the video information (real time signal) on graphics, non real time signal (second pre-processed video).

Considering claims 15 and 31, the claimed wherein the pre-processing includes addressing on a frame-by-frame basis the video signal being pre-processed which is met by the description at column 4, lines 28-36, whereas the addressing unit provide the memory addressing function while a displayable video information is known to be reference as frame by frame manner.

Considering claim 16, the claimed wherein the system in Peripheral Component Interconnect circuit board which is met by the description at column 3, lines 24-29.

Considering claims 17, 19, 20, and 22-24, the method claim recite the functional steps that are similarly recited in their correspond apparatus claims 1,3,4, and 6-8. Thus claims 17, 19, 20 22-24 are rejection for the same reason as applied to their respectively apparatus claims above.

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Considering claim 32, Wang et al. multiple pipeline memory controller for servicing real time data. Wang et al. discloses the following limitations a video input system for preprocessing video signals, note:

- a) the claimed video input system for pre-processing video signals which is met by the video graphic controller VGC 26 with a multiple pipeline (Fig. 2, column 3, lines 24-26 and lines 38-43);
- b) the claimed means for receiving one or more live video signals which is met by the video capture controller 38 (Fig. 2, column 3, lines 38-43), whereas a receiving means is inherently included for receiving the transmitted CATV signals;
- c) the claimed means for forwarding one or more live video signal, the video input module producing a forwarded video signal for each received live video signal which is met by the video capture controller 38 (Fig. 2, column 3, lines 38-43);
- d) the claimed means for pre-processing VS₁, wherein VS₁ is a first stored video signal or one of the forwarded video signals produced in the video input module, the first video pipeline producing a first pre-processed video signal which is met by the pipeline processor 68 (Fig. 3, column 4, lines 5-9, column 3, lines 60-65), whereas passage from column 4 describes pipeline processor 68 receives and processes the real time input signal from port 64, while the passage from column 3 additionally describes that the real time signal (VS₁) at port 64 which is the video capture signal originated from the video capture controller 38 (video input module); and
- e) the claimed means for pre-processing Vs2, wherein Vs2 is the same video signal being pre-processed in the first video pipeline, one of the other forwarded video signals

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produced in the video input module, or a second stored video signal, the second video pipeline producing a second pre-processed video signal which is met by the other dual pipeline processor 70 (Fig. 3, column 4, lines 2-15, column 3, lines 54-58), whereas the excerpt from column 4 describes that an non-real time signal is input thru the input port 66 to the other dual pipeline processor 70, while excerpt from column 3 describes that the input non-real time signal is generated by the GUI engine and retrieved from the accesses memories (a second stored video signal).

Claim Rejections - 35 USC § 103

- 2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 3. Claims 2, 18, and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. '906 in view of Wang '325.

Considering claims 2 and 33, Wang et al. discloses the claimed invention except for the claimed ancillary data extractor, the extractor removing ancillary data from at least one of the live video signals converted in the video input module as recited in claim 2, and the claimed means for removing ancillary data from at least one of the live video signal prior to converting the at least one live video signal as recited in claim 33.

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It is note that Wang et al. '906 discloses a video capture controller that receives the broadcasted live video signal (Fig. 2). Nonetheless, Wang '325 discloses a single port video capture circuit. Wang discloses the claimed ancillary data extractor or means for removing ancillary data, the extractor removing ancillary data from at least one of the live video signals converted in the video input module which is met by the video parser 20 that extract the VBI ancillary data(Fig. 1, column 2, lines 32-41 and lines 47-64).

Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to implement the system of Wang et al. with the teaching of Wang accordingly in order to facilitate the reception of VBI embedded ancillary signal such as closed caption data or secondary audio or digital data that is immanently part of the broadcast television, and rendering the system to fully utilize the embedded ancillary signal for their intended function.

Considering claim 18, the claim recites the functional method step with corresponding limitation as appears in the apparatus claim 2 above. Thus claim 18 is rejected for the same reason as applied to claim 2 above.

4. Claims 5 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. '906.

Considering claims 5 and 21, Wang et al. discloses the claimed invention except for the claimed limitation of wherein at least one of the pre-processed video signal is e-VS, wherein e-VS is an RGB encoded video signal, ... or a YUVA-Type encoded video signal.

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Wang et al. teaches the processed is video signal received and output thru a CRT controller 46 the received display data on screen through display bus (column 3, lines 45-49).

Examiner takes Official Notice that it is notoriously well-known in the art to provide an RGB or YUV encoded video signal as the processed video signal for outputting and displaying on the CRT, whereas the common CRT is known to be driven by RGB or YUV type of color signal.

Therefore it is submitted that it would have been obvious to one having ordinary skill in the art at the time the invention was made to implement the Wang et al. accordingly in order to render the display of the processed video signal on the color CRT display.

5. Claims 9-14, and 25-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. in view of Barilovits et al. (Pub.No. '610).

Considering claims 9-14, and 25-30, Wang et al. discloses the claimed invention except for the claimed limitation of wherein the process of pre-processing includes changing the sample rate, gamma removal, gamma insertion, color space conversion, and dithering, as recited in claims 9-14 respectively.

Nonetheless, Barilovits et al. discloses a video processing engine overlay filtering scaler. Barilovits et al. discloses the claimed pipeline processing includes the changing the sample rate, gamma removal, gamma insertion, color space conversion, and dithering which is met by the description at page 3, paragraph 0025-0036, whereas paragraph 25 describes that video processor implemented as pipeline machine that has the upsampling and down sampling

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function (sample rate changing), while paragraphs 0027-0036 describes the video processing includes gamma correction, color space conversion, and dithering (color promotion).

Since Barilovits et al. teaches such implementation of video processing including the about various processing that has the advantage better able to meet the feature requirement of a computer graphic system while simplifying the design (paragraph 0024, lines 1-5).

Therefore the examiner submits that it would have been obvious to one having ordinary skill in the art at the time the invention was made to implement the teaching of Barilovits et al. in the system Wang et al accordingly for the stated advantage.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Tenenbaum et al. discloses a video stream processing system.

Bowen et al. discloses a method and apparatus for synchronizing graphic pipelines.

Silverbrook discloses a real-time processing system for animation images to be displayed on high definition television systems.

Deming et al. discloses a multi-processor graphics accelerators.

Voltz et al. discloses an apparatus for providing video resolution compensation when converting one video source to another video source.

Kajiya et al. discloses a method and system for rendering graphical objects to image chunks.

Newman et al. discloses a media editor for non-linear editing system.

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Gardyne et al. discloses a system and method for performing motion estimation with reduced memory loading latency.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linus H. Lo whose telephone number is (703) 305-4039.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John W. Miller, can be reached at (703) 305-4795.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

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December 14, 2002

IOHN MILLER

SUPERVISORY PATENT EXAMINER TECHNOLOGY CENTER 2600